Process, Design and Material Factors for Voiding Control for Thermally Demanding Applications

Amit Patel, Matthew Siebenhuhner, Gyan Dutt, Ranjit Pandher, Mitch Holtzer, and T.W. Mok
Alpha Assembly Solutions
South Plainfield, NJ, USA
Amit.Patel@alphaassembly.com

ABSTRACT
Solder voiding is a common phenomenon across all semiconductor packaging and electronic board assemblies. Voids are a troublesome defect in assemblies created using surface mount technology. Voids can interfere with electric signals, can be insulators when heat dissipation is required, and they can also be the source of crack propagation and early failure of an assembly when occurring near the pad surface. The acceptable levels for voiding vary upon on the end-application and environment it's used in. In the case of thermally demanding harsh environment applications such as automotive and outdoor LED lighting void control is required in order to optimize the performance and extend the lifetime of these components. The lower the voiding on these thermal and electrical pads, the better the connection to the PCB and subsequent layers.

There are many factors that influence void frequency and size. This study focuses on several process, design and materials selection considerations which control or potentially reduce voiding to meet industry and end-market acceptance criteria. More specifically, package design, reflow profiles, and solder paste chemistry are discussed in the form of application studies. Commercial mid-power PLCC and high-power ceramic LED packages on aluminum metal core PCBs additionally BGA, D-Pak, and MLF on FR4 PBCs were used for these case studies.

Key words: LED, Voiding, Thermal Management, Lifetime, Reliability, Solder Paste, Alloy, LED Package

INTRODUCTION
The global acceptance of LED-based light sources has propelled the energy efficient technology to enter numerous markets and end applications including high power lighting segments. Examples include exterior automotive headlamps, roadway/street lighting, industrial high bay lights, architectural and entertainment lighting. As a result, customer expectations of maintaining efficiency, government regulations, safety, and reducing overall systems / replacement costs are important to satisfy the adoption rates.

For these high reliability and lifetime requirements, it is critical to have excellent assembly interconnect reliability to address the above needs.

The role of interconnects in LED Level 1 (chip /die attach) and Level 2 (package on board attach) is fundamentally to:

- Convey power and information efficiently and reliably over the rated life.
- Thermal management - get the heat out faster and reliably over the rated life.
- Enable more light output, consistently, for longer time for the same package and system footprint.
- Capable of being processed under robust processing conditions i.e. multiple reflow assembly.

Voids, which are pockets of trapped gasses from solder flux, can cause issues for electric signals, can act as thermal resistors when heat dissipation is required, and they can also be the source of crack propagation and early failure of an assembly. Figure 1 depicts large area voids in the bulk solder layer. The phenomenon of void occurrence is a complex system, there are many factors that drive various levels of voiding. Examples include: chemistry, reflow profile, volume of material, solderable pad finish and design of the component pads (thermal and electrical).

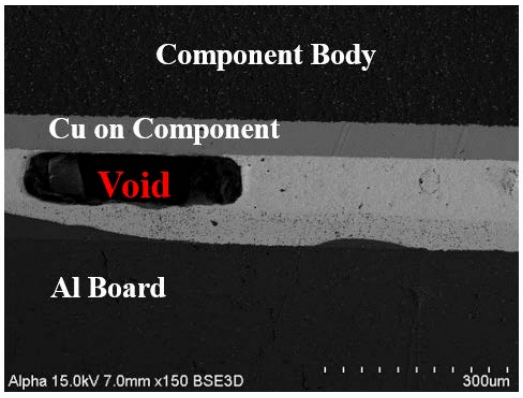

Figure 1. Voids Entrapment within the Solder Layer

For level 1 LED chip attach assemblies the use of traditional solders can be seen as an advantage from both ease of processing and cost. However, the importance for thermal management is critical for high and ultra-high power LEDs. The junction temperature in the LED increases with increasing drive current. Since more than 50 % of electrical input power is dissipated as heat due to efficiency droop at high drive currents in LEDs, this rise in the junction temperature reduces the light output by increasing the probability of non-radiative recombination causing drop in efficiency and rated lifetime. Therefore, the dissipated heat needs to be removed from the junction in order to maintain the light conversion efficiency and light output from the High Power LED package. The various components in the heat flow path in a High Power LED package are shown in Figure 2.

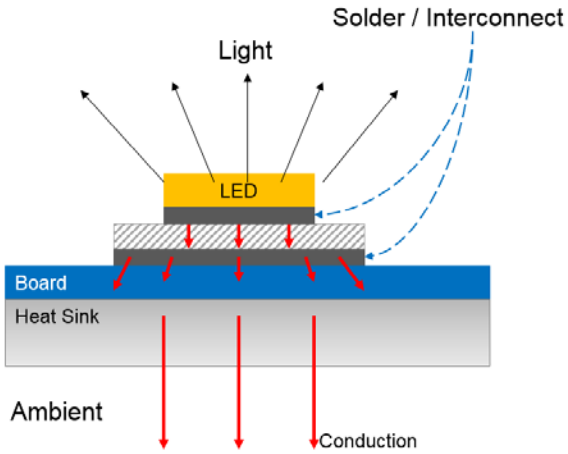

Figure 2. High Power LED Heat Path.

Additionally for Level 1, the requirements for processing LED packages with solder based die attach on boards as a Level 2 assembly requires multiple soldering reflow capability. With multiple reflows of the same solder bulk layer may increase the levels of voids impacting the overall reliability of the stack at the Level 1 layer.

For Level 2 package on board assemblies LEDs are becoming more integrated with various traditional IC components such as BGAs, D-Paks and MLFs being directly mounted on the same board. This is driven by the need for lighting systems to go beyond general illumination providing more complex features such as control, sensing and modulation. Large area voids can create issues in the electrical signal or generate cracks due to thermal cycling / fatigue thus need for a more robust, low voiding interconnects are required at the Level 2 layer.

EXPERIMENTAL PROCEDURE – DESIGN CASE

There are a variety of LED designs used in the industry ranging from design structure / size and package materials i.e. ceramic and plastic. The goal of this experiment is to observe the effect of voiding based on 3 varying structures with the key difference being the pad geometries. For example, a 2 pad design where the anode and cathode are symmetrical, a 3 pad high aspect ratio design where the central thermal pad is slightly larger in terms of total area and lastly, a 3 pad design where the central thermal pad is significantly larger in terms of total area when compare to the anode and cathode. Table 2 shows the total area and construction of the LED pads.

ASSEMBLY MATERIALS & COMPONENTS

Substrate

The substrate used in this study is a custom designed aluminum core PCB. The particular details for this board are shown in Table 1.

Details	Metal Core PCB
Metal Core	Aluminum
Surface Finish	ENIG

Table 1. Test Vehicle Details

LED Components

For this study, three commercially available high power LEDs were selected with varying pad geometries. The parameters for anode, cathode, and thermal pad dimensions for the LEDs are listed in Table 2. All dimensions are in millimeters. The LEDs were chosen to emulate common packages selected in high and ultra-high power assemblies.

LED Design	Anode (mm)	Cathode (mm)	Thermal Pad (mm)
LED A	1.35 x 3.2	1.35 x 3.2	N/A
LED B	0.5 x 2.7	0.5 x 2.7	1.0 x 2.7
LED C	1.2 x 0.67	1.2 x 0.67	1.77 x 2.80

Table 2. LED Pad Dimensions (mm)

Solder Pastes

A commercially available no-clean solder paste was used for this study known using a type 4[1] particle size SAC-based alloy.

PROCESS AND TEST METHOD

Equipment Processing Details

Solder paste printing was done using DEK Horizon 03iX printer with a 4 mil thick laser cut stainless steel stencil with a 1 to 1 ratio of aperture size to pad size. Stencil printing parameters used for all solder pastes are shown in Table 3.

SMT Parameters	Process Conditions
Print Speed	1 inch/sec.
Print Pressure	1.25 lbs/inch of blade
Stencil Release	0.02 inches/sec.
Stencil Thickness	4mil

Table 3. Print Conditions

Reflow Soldering

The soak reflow profile was used in this study shown in Figure 2 the temperatures are displayed in Table 4.

[1] 38–20 Particle size in µm (80% min. between)

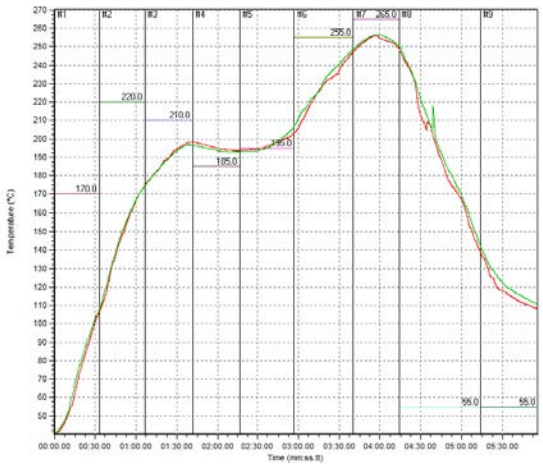

Figure 2. Reflow Profile, Visual Depiction

Line Speed:	Zone:	#1	#2	#3	#4	#5	#6	#7	#8	#9
23.000 (in/min)	Length (in):	12.60	12.99	13.50	13.31	15.39	16.61	12.99	22.99	16.02
	Upper (°C):	170.0	220.0	210.0	185.0	195.0	255.0	265.0	55.0	55.0
	Lower (°C):	170.0	220.0	210.0	185.0	195.0	255.0	265.0	55.0	55.0

Table 4. Reflow Profile used in study

Test Method

To measure and quantify the voiding performance of the varying pastes and LED pad layouts, the assembled and reflowed boards were loaded into an X-ray analysis unit and programmed to quantify the area of each void as a percent of the total pad area and the number of voids under the package.

RESULTS AND DISCUSSION

Results

The results of this study are shown in Figure 4.

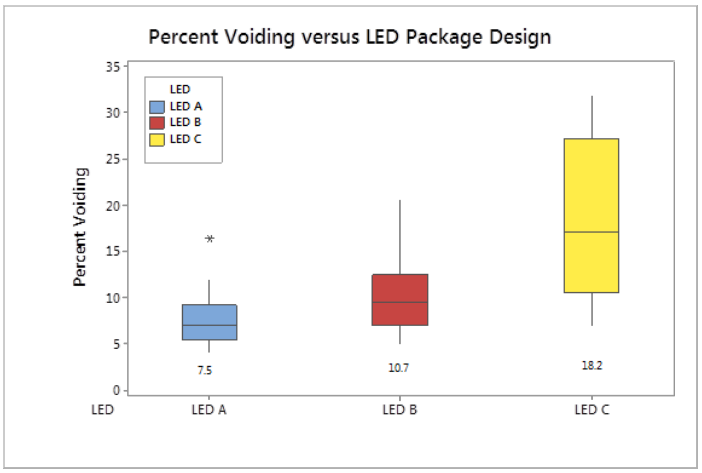

Figure 4. Percent voiding versus LED package design.

Discussion

From the experimental results, it is evident that solder pad design influences the level of voiding for a given package. The selected packages which have the largest physical difference of pad area and asymmetry in design creates the highest levels of voiding. This is directly related to the total volume of solder deposit for a particular LED package. Table 5 depicts the pad variance for a given design.

LED Design	Anode (mm)	Cathode (mm)	Thermal Pad (mm)	Difference in Thermal Pad vs. Electrical Pad (mm2)
LED A	1.35 x 3.2	1.35 x 3.2	No Pad	0
LED B	0.5 x 2.7	0.5 x 2.7	1.0 x 2.7	1.35
LED C	1.2 x 0.67	1.2 x 0.67	1.77 x 2.80	4.15

Table 5. LED Design Dimensions and Difference in Thermal vs. Electrical Pads

It is known that having different solder volumes on the same board makes it very difficult to adjust reflow profile setting that balances the activation and evaporation component. A small volume consumes the activator faster than a larger volume which requires a much longer soak profile to remove the diluents / solvents in the flux system.

EXPERIMENTAL PROCEDURE – PROCESS CASE [1]

Adjusting the reflow profile is a very common starting point in order to optimize the level of voiding. In the first set of experiments, multiple solder paste formulations were subjected to various reflow profiles. The profile variations included preheat soaks, and time above liquidus. All reflow profiles were created using a seven zone convection oven using no nitrogen. An in-house developed test vehicle, based on a .062 thick FR4 laminate, finished with OSP/Copper pads was used. The test vehicle includes BGA, D-Pak, and MLF devices.

Test Method

Voiding was measured with a Nikon Metrix XT V160 2-D x-ray machine. In each case, altering the profile had an effect on the observed level of voiding.

Varying the Preheat Profile

Two reflow profiles with different preheat settings. The first is known as a straight ramp profile, where the test vehicle's surface temperature increases at a near linear rate of +1.5°C per second up to a peak temperature if 245°C. The second profile has a slightly faster ramp up (+1.56°C/second) to approximately 160°C, then the assembly is allowed to "soak" at temperatures between 160°C and 184°C for approximately 60 seconds, followed by a moderate (0.96°C/second) ramp up to a peak temperature of 240°C.

RESULTS AND DISCUSSION

Results

Figure 5 shows the effect the two reflow profiles on a BGA 256 device using one solder paste. Both the solder paste alloy and the BGA spheres were made with SAC 305 alloy.

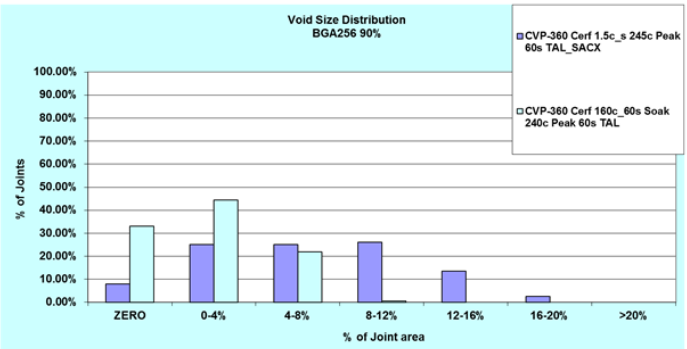

Figure 5. Voiding Results

Discussion

The soak profile resulted in over 30% of the 265 BGA I-Os having no voids. With the straight ramp profile, fewer than 10% had zero voids. The soak profile had zero BGA joints with more than 8% by area, voiding, whereas over 10% of the straight ramp profile results had voids between 12% and 16% of the area. The result of adding a preheat soak and a slower ramp rate to the peak temperature significantly reduced the extent of voiding in BGA components when compared to a fast ramp to peak temperature.

Extending Time Above Liquidus

Another adjustment to the reflow profile that has proven to reduce voiding is extending the time above liquidus. This is especially effective with large surface area components like MLFs, DPAKs, TO-252 and other bottom terminated components (BTCs).

In order to verify the effect the impact of extending the time above liquidus the concept was captured on video using a reflow simulation.

Test Method

A solder paste deposit was placed on a large metalized surface. A piece of glass was placed over the deposit. The video camera captured the image of the solder paste as it went through a reflow profile. Images were captured at key temperatures of the reflow profile to explain the formation and elimination of voids.

RESULTS AND DISCUSSION

Results

The formation of gas bubbles from the evaporation/boiling of organic solvents can readily be observed. This outgassing before the alloy reaches liquidus is an explanation for the reduced levels of voiding seen when a soak preheat profile replaces a straight ramp preheat. A greater volume of the gas producing solvents are driven off before the solder spheres melt and coalesce in a liquid phase; see Figure 6.

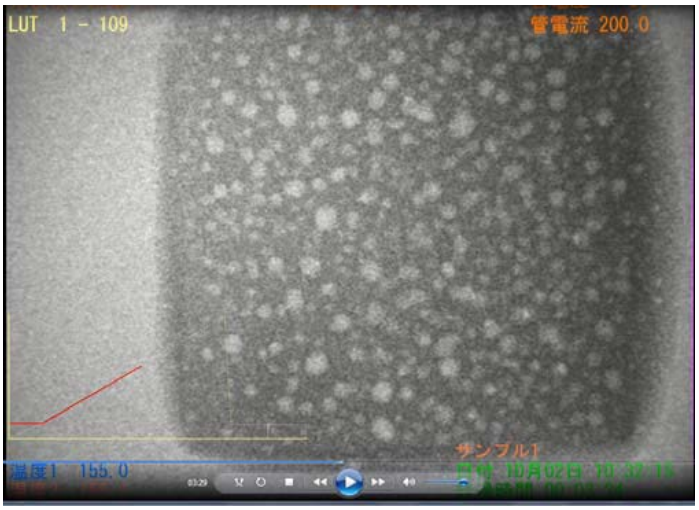

Figure 6. Outgassing During a Straight Ramp Reflow Profile @ 155°C

For the next stage of the profile the voiding changes noticeably; see Figure 7.

Figure 7. Large Voids Photographed as Solder Reaches Liquidus

Rather than the smaller, yet high frequency voids seen at 155C now there are much larger pockets of gas between the component and board. If the solder is allowed to freeze the pockets will remain in the bulk solder. While the component/solder/board stack up shown in Figure 7 is above the liquidus temperature of the solder, the vapor bubbles are mobile due to Brownian motion forces caused by the heat input from the reflow simulator. If these air pockets reach the outer boundary of the top component, the gas is released and the void disappears. Once the void disappears, there is no source of new gas entrapment (as long as the peak remains below 242°C in the presence of copper). This is how an extended time above liquidus can greatly reduce the amount of voiding under a bottom terminated component. Figure 8 shows this result.

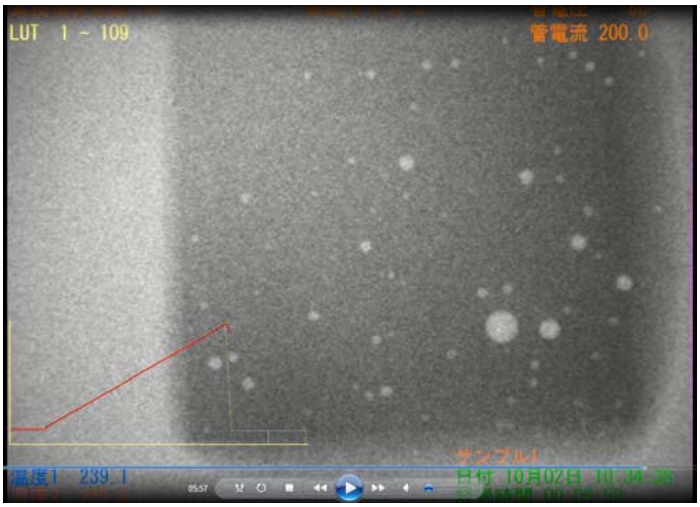

Figure 8. Reduced Voiding After Extended Time Above Liquidus

Discussion

Adjusting the reflow profile is a very easy way to reduce voids. Using a soak pre-heat profile reduces voiding in BGA devices. Keeping the peak temperature below 241°C reduces voiding in BGA and BTC components. Increasing the time above liquidus reduces voiding in BTCs as well.

EXPERIMENTAL PROCEDURE – CHEMISTRY CASE

Solder paste chemistry is a highly proprietary subject. However, there is significant experimental evidence that shows the presence or absence of various useful ingredients in solder paste do have a major influence on voiding this example can be seen in Figure 9. The following case looks at two solder paste chemistries and its impact of voiding under the same the process and conditions.

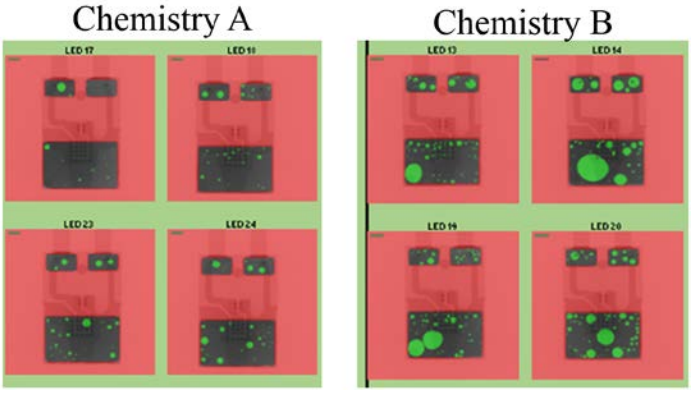

Figure 9. Difference in Solder Chemistries vs. Voiding

ASSEMBLY MATERIALS & COMPONENTS

Substrate

The substrate used in this study is a custom designed aluminum core PCB. The particular parameters for this board are detailed in Table 6 below. The pad dimensions of the substrate are listed in

Parameters	Metal Core PCB
Metal Core	Aluminum
Surface Finish	HASL

Table 6. Test Vehicle Details

LED Components

For this study, a commercially available ceramic LED was selected. Details of the LED are show in Figure 9.

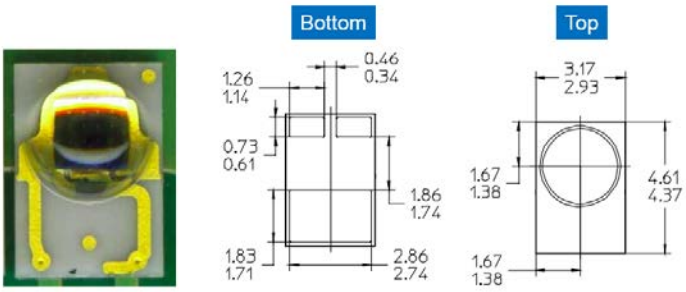

Figure 9. Commercially Available Ceramic LED Package

Solder Pastes

Two commercially available no-clean Lumet solder pastes were used. Paste A has been formulated from the ground up to deliver low voiding while Paste B served as the standard control.

PROCESS AND TEST METHOD

Equipment Processing Details

Solder paste printing was done using DEK Horizon 03iX printer with a 4 mil thick laser cut stainless steel stencil with a 1 to 1 ratio of aperture size to pad size. Stencil printing parameters used for all solder pastes are shown in Table 7.

SMT Parameters	Process Conditions
Print Speed	1 inch/sec.
Print Pressure	1.5 lbs/inch of blade
Stencil Release	0.02 inches/sec.
Stencil Thickness	5mil

Table 7. Print Conditions

Reflow Soldering

Using the learnings from the Process Case a soak reflow profile was generated the conditions are 180-200C/90s Soak 255C Peak 80s TAL Figure 10 shows the profile.

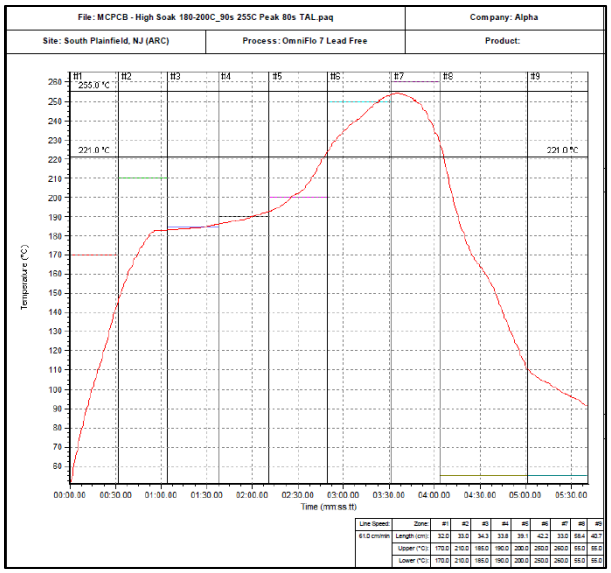

Figure 10. Reflow Profile, Visual Depiction

Test Method

To measure and quantify the voiding performance an X-ray analysis unit was programmed to quantify the area of each void as a percent of the total pad area and the number of voids under the package. Figure 11 shows the areas under study.

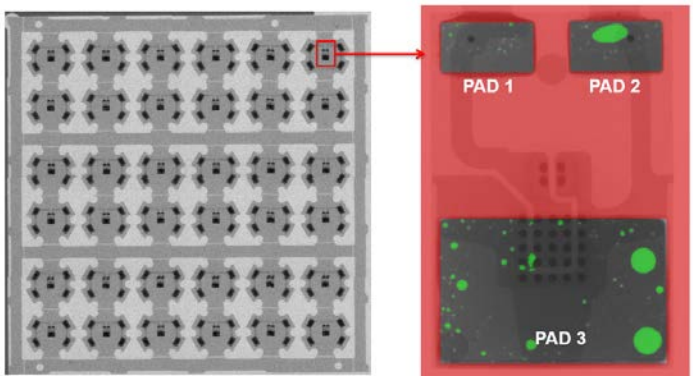

Figure 11. X-Ray Image of Soldered Ceramic Based LED Package

RESULTS AND DISCUSSION

Results

The results of this study are shown in Figure 12 and Table 8.

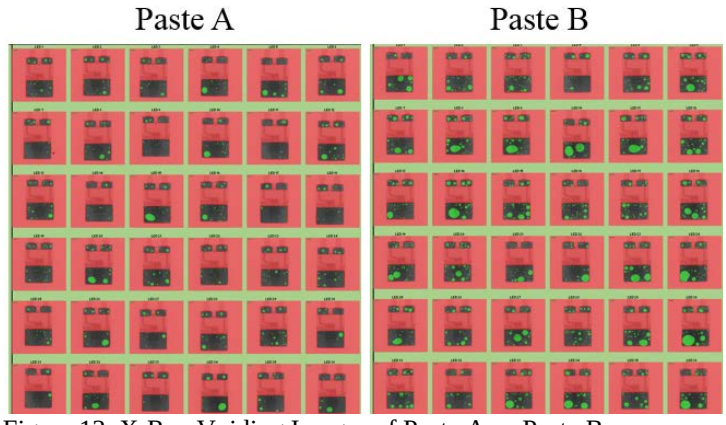

Figure 12. X-Ray Voiding Images of Paste A vs Paste B

Paste	Sample Size (N)	Avg. Number of Voids	Total Void Per Area (%)
Paste A	N = 72	57	10
Paste B	N = 72	92	19

Table 8. Voiding Size and Frequency

Discussion

Paste A indeed provides better voiding under the same processing conditions. Paste A produced 40 percent lower number of physical voids and provided an average of 9 percent voiding per total area when compare to 19% for Paste B. The presence or absence of various useful ingredients exist for both Paste A and Paste B which can impact voiding in either direction as seen in the results. As a general guideline it is important to understand the trade-offs between a pastes that delivers low voiding and the other paste characteristics that could be impacted. This decision will be dependent on the acceptable voiding criteria for a given application / customer requirements.

CONCLUSIONS

Voids are an area of concern for the long term durability and functionality of electronic devices. Voids near or at the interface of surface mount technology (SMT) component input/outputs (I/O's), or the circuit board substrate can be highly probable initiators of crack propagation, leading to the high possibility of a field failure. Also, voids are very good insulators of heat, leading to thermal issues with heat sinks and thermal pads often used in LED packages.

There are many factors that influence void frequency and size. This study showcases serval design, process and chemistry impact on voiding.

There are many drivers for LED designs today. Particularity the design of solder pads both influences the thermal, electrical and mechanical characteristics of the LED package. The impact of pad symmetry which is directly related to total solder volume can influence the voiding performance.

Adjusting the reflow profile is a very easy way to reduce voids. Using a soak pre-heat profile reduces voiding in BGA devices. Increasing the time above liquidus reduces voiding in BTCs as well.

Solder paste chemistry also has a significant effect on voiding.

REFERENCES

1. M. Holtzer, T.W. Mok, "Methods of Reducing or Eliminating Voids in BGA and BTC Devices" SMTA Penang – MY March 2016.